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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/817,843
Filing Date: March 26, 2001
Appellant(s): KNICKERBOCKER ET AL.

John A. Evans
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed September 07, 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 1-3, 17-21 and 35-37 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

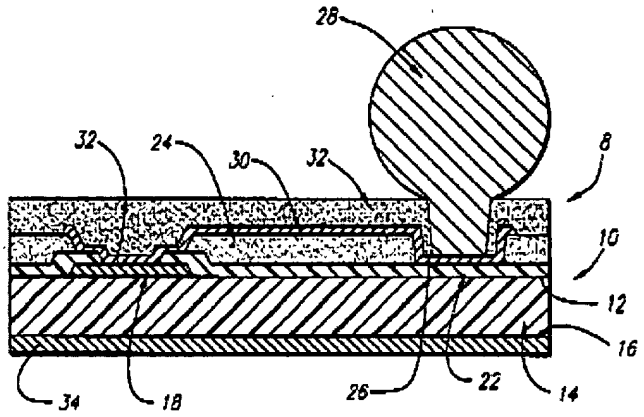
6,441,487	Elenius et al.	8-2002
6,204,454	Gotoh et al.	3-2001

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-3 and 17-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Elenius et al. (US 6,441,487).

Regarding claim 1, Elenius (e.g. figs. 1 and 2) shows an electronic package comprising: a dielectric packaging substrate 22 having a major surface (top surface); and a conductive foil 30 having a smooth portion. The conductive foil is laminated with the substrate major surface. Also, the smooth portion (bottom) contacts the major surface of the dielectric packaging substrate.



Regarding claim 2, Elenius discloses that the conductive foil may comprise aluminum, nickel or copper (col. 7/lls. 1-28).

Regarding claim 3, Elenius discloses that the conductive foil may comprise a high electrical conductivity material such as aluminum, nickel, titanium or copper (col. 7/lls. 1-28).

Regarding claim 17, Elenius (e.g. figs. 1 and 2) shows an electronic package comprising: a semiconductor packaging substrate 12 having a major surface; a first mechanically compliant dielectric layer 22 formed over the major surface of the substrate and having a at least one first opening formed therethrough; a first electrical contact pad 18 formed in the first opening and in electrical contact with the substrate; a second mechanically compliant dielectric layer 24 formed over the first compliant layer and having at least one second opening formed therethrough wherein the second opening is substantially offset from the first opening; a second electrical conductive pad 30 formed in the second opening and extending over a portion of the first electrical contact pad and contacting the first electrical contact pad; a mask layer 32 formed over the second compliant layer and having a third opening therethrough in communication with the second electrical contact pad; and a solder ball 28 solderably connected to the second electrical contact pad and extending through the third opening.

Regarding claim 18, Elenius shows that the mask is a solder mask.

Regarding claim 19, Elenius shows that the compliant layers can be made of benzocyclobutene. Benzocyclobutene is a photoresist material (e.g. US 6,361,926, col.1/lls. 56-59).

Regarding claim 20 and 21, Elenius discloses that the contact pads may comprise aluminum, nickel or copper (col. 7/lls. 1-28).

Claims 35-37 are rejected under 35 U.S.C. 103(a) as being obvious over Elenius et al. (US 6,441,487) in view of Gotoh et al. (US 6,204,454).

Regarding claims 35 and 36, Elenius shows most aspects of the instant invention including a contact pad laminated surface adhesion. However, Elenius does not disclose the specific roughness of the conductive surface. Gotoh discloses a conductive foil having a roughness in a range of 0.3 to 0.5 microns (col. 7/lls. 9-11). Gotoh discloses that this type of embodiment improves the electrical connection stability (col. 5/lls. 34-41). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make conductive surface disclosed by Elenius having a roughness in a range of 0.3-0.5 microns in order to improve the electrical connection stability as suggested by Gotoh.

Regarding claim 36, Elenius in view of Gotoh does not disclose that the roughness is less than 0.01 microns. However, the specific roughness claimed by applicant, i.e., less than 0.01 microns, absent any criticality, is only considered to be the "optimum" roughness value of the conductive surface disclosed by the Prior Art that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired accuracy, manufacturing costs, etc. (see In re Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, i.e., results which are different in kind and not in degree from the results of the prior art, will be obtained as long as an opening in the housing is used as already suggested by the Prior Art. Note that Gotoh suggests that the surface roughness is a variable that can be subjected to optimization (cols 4-7).

(11) Response to Argument

ARGUMENT A

Applicant argues:

Elenius fails to anticipate the present invention because Elenius is silent as to a conductive foil having a smooth side.

Examiner responds:

Initially, it is respectfully noted that the term "smooth" is interpreted in light of the specification as a plane surface that does not have dendrites (see e.g. page 3/lines 1-7 of applicant's specification). In that regards, Elenius' fig. 2 (see above) teaches a copper foil 30 having a top and bottom surfaces not having dendrites. Elenius' fig. 2 clearly anticipates the claim invention in accordance to the given interpretation. Also, the term "smooth" is a relative term and not an absolute term as suggested by applicant. For example a paper sheet is smooth if is compared with a polish pad but it is not smooth if it is compared to silk.

Applicant argues:

Examiner explicitly acknowledges the failure of Elenius to teach a smooth surfaced foil. In the Final Office Action, mailed May 5, 2004, in the context of making a rejection under 103, the Examiner states: "However, Elenius does not disclose the specific roughness of the conductive" Not only does Elenius fail to disclose a specific roughness of the conductive foil; surface indeed, Elenius fails to disclose that one side of the foil must be smooth.

Examiner responds:

The fact that Elenius does not disclose the specific surface roughness value of the conductive foil does not imply that surfaces are not smooth. As stated above the term "smooth" is interpreted in light of the specification as a plane surface that does not

has any dendrites an not in term of a specific roughness value. Therefore, it would be improper to interpret the term "smooth" in terms of a roughness value when neither the claims nor the specification do so. The fact that Elenius' foil surfaces are plane and do not include any dendrites cannot be ignored. In that context, any plane surface must be considered "smooth" as long it does not have any dendrites. If a prima facie case of anticipation is established, the burden shifts to the applicant to come forward with arguments and/or evidence to rebut the prima facie case. See, e.g., Dillon, *919 F.2d at 692, 16 USPQ2d at 1901*. Rebuttal evidence and arguments can be presented in the specification, *In re Soni, 54 F.3d 746, 750, 34 USPQ2d 1684, 1687 (Fed. Cir. 1995), by counsel, In re Chu, 66 F.3d 292, 299, 36 USPQ2d 1089, 1094-95 (Fed. Cir. 1995)*, or by way of an affidavit or declaration under 37 CFR 1.132, e.g., Soni, 54 F.3d at 750, 34 USPQ2d at 1687; In re Piasecki, 745 F.2d 1468, 1474, 223 USPQ 785, 789-90 (Fed. Cir. 1984). However, arguments of counsel cannot take the place of factually supported objective evidence. See, e.g., *In re Huang, 100 F.3d 135,139-40, 40 USPQ2d 1685, 1689 (Fed. Cir. 1996); In re De Blauwe, 736 F.2d 699, 705, 222 USPQ 191, 196 (Fed. Cir. 1984)*.

ARGUMENT B

Applicant argues:

Elenius fail to anticipate the present invention because Elenius does not laminate a conductive foil to a "*substrate*" because the element 22 is a wafer passivation layer and not a substrate. Applicant argues that substrate for the instant art is a wafer.

Examiner responds:

Although the term substrate may be defined as wafer this term is not exclusively restricted to a wafer. In the instant case, the term substrate is interpreted as "underlying layer" which is the broadest reasonable interpretation (see definition attached to the final rejection sent on May 5, 2004). Furthermore, this interpretation is commonly used in the semiconductor art and is in accordance with applicant's specification. For example, applicant discloses that the dielectric substrate might be a single or multilayer dielectric (page 3/lines 4-8 and fig. 1). Therefore, a single dielectric layer can be considered a substrate in accordance with the ordinary meaning and with applicant specification. Moreover, the definition attached to the appeal brief filed on September 09, 2004 is incompatible with the meaning given by claim 1 because the submitted definition define the term substrate as to be a wafer whereas the claim recites a dielectric substrate. By definition a wafer is "a thin slice of semiconductor material" (see technical definition attached to this document). These definitions are mutually exclusive because a dielectric material does not conduct electricity whereas a semiconductor may conduct.

Applicant argues:

The Examiner equates the redistribution trace 30 of Elenius with the "conductive foil" recited in claim 1. Claim 1 requires that the conductive foil be laminated to said major surface of the substrate. By contrast, Elenius' redistribution trace 30 is formed over the wafer passivation layer 22, and is not laminated to a major surface of the wafer 14. The invention recited in claim 1 therefore differs from Elenius and the rejection is improper.

Examiner response:

As stated above a dielectric underlying layer such as the passivation layer 22 disclosed by Elenius can be recognized as a dielectric substrate. Therefore, Elenius properly anticipate the claim invention because the "conductive foil 30" is laminated over the passivation layer which is in fact a dielectric substrate.

ARGUMENT C

Applicant argues:

The Examiner states explicitly that Elenius is silent as to a foil having a smooth side. The Examiner cites Gotoh as teaching roughening a foil to provide surfaces roughness in specified ranges. However, Gotoh does not complete the teaching of Elenius because Gotoh does not teach a smooth side.

Examiner responds:

As stated in the response of argument A, Elenius explicitly teaches a conductive foil 30 having smooth surfaces.

ARGUMENT D

Applicant argues:

The Examiner acknowledges that Elenius is silent regarding the surface roughness of the foil. The Examiner cites Gotoh as teaching surface roughness. However, the cited art fail to provide incentive for the proposed combination. As the Examiner acknowledges, Gotoh relates to methods to increase the stability of an electrical connection. However, the present invention is directed at a means of decreasing the stability of the connection. Gotoh specifically teaches away from the present invention. Teaching away" from the invention is a "*per se* demonstration of nonobviousness.

Examiner responds:

Applicant argues that Gotoh teach away form the invention. Nonetheless, Gotoh provide positive motivations. For example, Gotoh discloses that this type of embodiment improves the electrical connection stability (col. 5/lls. 34-41). The fact that applicant has

recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985). Applicant argues that the present invention is directed at a means of decreasing the stability of the connection. Nevertheless, this statement is inconsistent with applicant specification. The present invention is directed to avoid a fracture of the solder connection (solder/pad connection) by reducing the adhesion of the pad to the laminate (see pp 0007). In other words, by reducing the adhesion of the pad to dielectric substrate the solder connection stability can be assured. Gotoh's teachings are not conflicting with Elenius teaching because the stability of the connection is achieved by increasing the adhesion of a metal-to-metal (i.e. pad to pad connection, see col. 3/lls. 34-45). In the instant combination, the top surface of the copper foil 30 was modify by making the top surface rough in order to increase the stability of the metal to metal connection comprised by the solder ball 28 and the pad 30 and not to increase the adhesion of the bottom surface of the pad 30 to the dielectric substrate 22 as suggested by applicant (emphasis added). Note that this is a metal to dielectric attachment.

ARGUMENT C

Applicant argues:

The legal standard for the prima facie case of obviousness requires that the cited art provide a reasonable expectation of success. Gotoh relates to methods of roughening a conductive foil and to the enhanced adhesiveness that such surface roughening provides. A person of skill would not look to the teachings of roughening foil to determine the properties of smooth foil. Gotoh fails to provide a reasonable expectation of success because Gotoh teaches away from the present invention.

Examiner response:

It is respectfully noted, that the cited combination provide a reasonable expectation of success since the provide teachings of Elenius and Gotoh suggest a device having an improved connection stability. Furthermore, there is not objective evidence in Elenius, Gotoh, and neither applicant's arguments that the cited references cannot be combined because it would result in an inoperative device. Since the teachings of Gotoh provide a positive motivation, are compatible and in the same art of endeavor of Elenius, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references by making the top surface of the conductive foil 30 disclosed by Elenius having a roughness in a range of 0.3-0.5 microns in order to improve the electrical connection stability as suggested by Gotoh.

For the above reasons, it is believed that the rejections should be sustained.

An appeal conference was held on November 10,2004 with Mr. Leonardo Andújar (Patent Examiner), Mr. Olik Chaudhuri (Supervisory Patent Examiner), and Mr. Nathan J. Flynn (Supervisory Patent Examiner), as the conferees.

Respectfully submitted,

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W

wafer a thin slice of semiconductor material on which semiconductor devices are made. Also called a slice or substrate.

wafer fab the facility (building) in which semiconductor devices are fabricated. Also called a semiconductor fabrication facility.

wafer scale integration most integrated circuits are cut from a large slice of material called a wafer. With wafer scale integration, the entire slice of material is used to create a complex circuit.

wafer sort a preliminary electrical test of each die while still on the wafer to eliminate most of the bad die before they are assembled.

wait state a bus cycle during which a CPU waits for a response from a memory or input-output device.

wall clock a device providing the time of day; contrast processor clock. Elapsed wall clock time for a process does not correspond with processor time because of time used in system functions.

Walsh cover mutually orthogonal sequences used in direct-sequence code division multiple access, obtained from the rows of a Hadamard matrix. *See also* Hadamard matrix.

Walsh transform *See* Walsh–Hadamard transform.

Walsh-Hadamard transform (WHT) a transform that uses a set of basis functions containing values that are either +1 or −1, and are determined from the rows of the Hadamard matrices. This has a modest decorrelation capability and is simple to implement.

Waltz filtering also termed "Boolean constraint propagation"; a method of simplifying certain tree-search problems. It was originally developed to solve the computer vision problem of labeling each edge of a line drawing in order to give a 3-D description of the represented object.

WAN *See* wide-area network.

Ward–Leonard drive an adjustable voltage control drive system for the speed control of DC machines, whereby variable voltage is supplied to the armature, while maintaining constant voltage across the shunt or separately excited fields. The variable voltage is obtained from a motor-generator set. The Ward–Leonard drive was frequently used in elevators.

warm start (1) reassumption, without loss, of some processes of the system from the point of detected fault.

(2) the restart of a computer operating system without going through the power-on (cold) boot process.

watchdog processor a processor that observes some process and signals an alert if a certain event happens or fails to happen.

watchdog timer a simple timer circuitry that keeps track of proper system functioning on the basis of time analysis. If the timer is not reset before it expires, a fault is signaled, e.g., with an interrupt.

water resistivity a measure of the purity of cooling liquid for a power tube, typically measured in megohms per centimeter.

water tree a microscopic cracking pattern

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